SPECIFICATION
FOR
EPD Module

MODULE No:	KD029QVFSN005
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2023.07.07	V1.0	ALL	FIRST ISSUE

Contents

1. Over View

KD029QVFSN005 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The 2.9inch active area contains 296×128 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label(ESL) System.

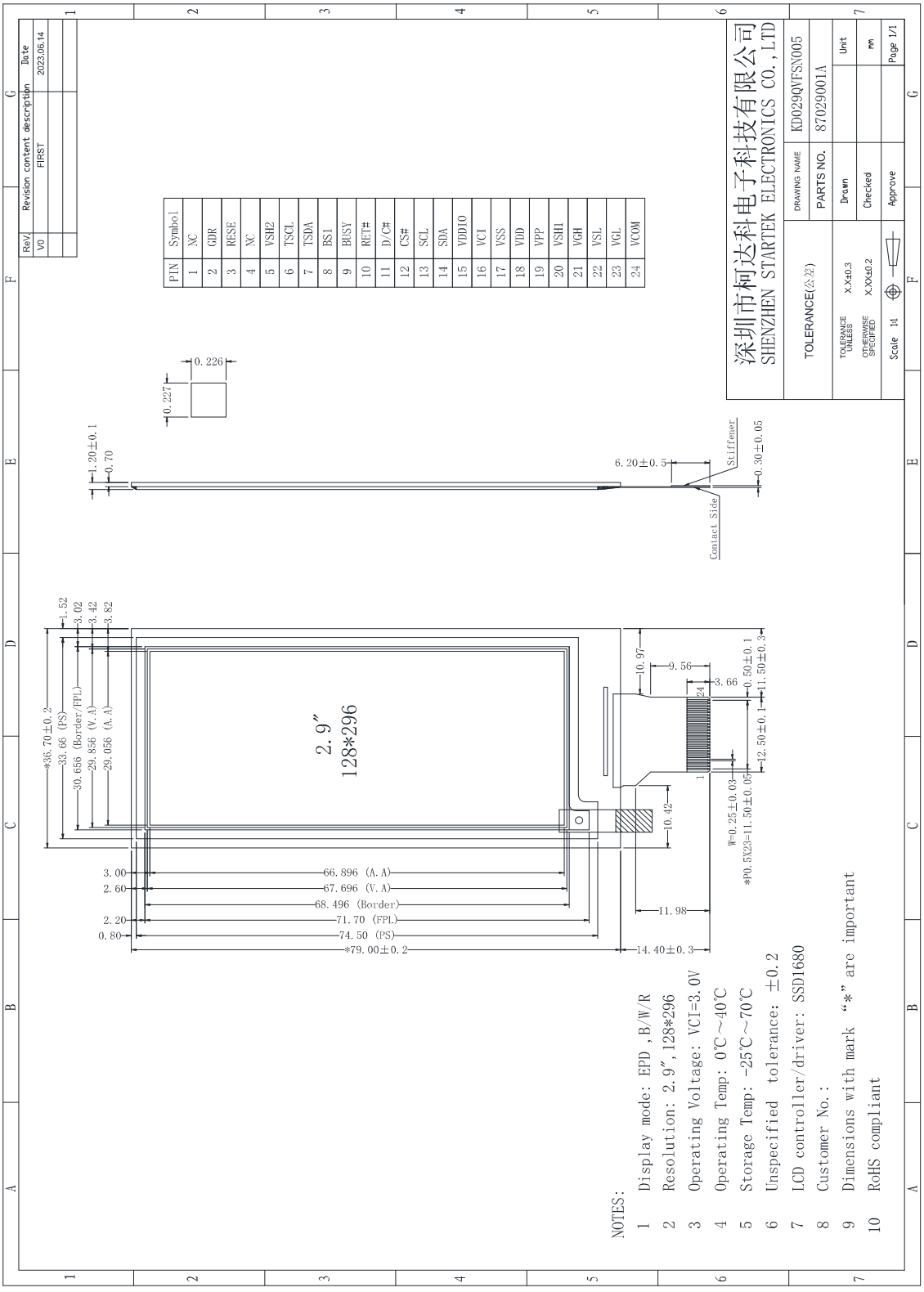
2. Features

- 296×128 pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor
- Built-in temperature sensor

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	128(H) x 296(V)	Pixel	
Active Area	29.056(H) x 66.896(V)	mm	
Pixel pitch	0.227(H) x 0.226(V)	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H) x 79.0(V) x 1.20(D)	mm	
Module Weight	6	g	
Controller IC	SSD1680		
Interface	3Wire / 4Wire SPI	-	
Display mode	EPD,B / W / R	-	
Operating temperature	0～+40	℃	
Storage temperature	-25～+70	℃	

4. Mechanical Drawing of EPD module



5. Input/Output Pin Assignment

NO.	Name	DISCRIPTION	I/O	Remark
1	NC	NO Connection	-	Keep open
2	GDR	N-Channel MOSFET Gate Drive Control	O	
3	RESE	Current Sense Input for the Control Loop	I	
4	NC	NO Connection	-	Keep open
5	VSH2	Positive Source driving voltage(Red)	C	
6	TSCL	IIC Interface to digital temperature sensor Clock pin	O	
7	TSDA	IIC Interface to digital temperature sensor Data pin	I/O	
8	BS1	Bus Interface selection pin	I	Note 5-5
9	BUSY	Busy state output pin	O	Note 5-4
10	RES#	Reset signal input. Active Low.	I	Note 5-3
11	D/C#	Data /Command control pin	I	Note 5-2
12	CS#	Chip select input pin	I	Note 5-1
13	SCL	Serial Clock pin (SPI)	I	
14	SDA	Serial Data pin (SPI)	I/O	
15	VDDIO	Power Supply for interface logic pins It should be connected with VCI	P	
16	VCI	Power Supply for the chip	P	
17	VSS	Ground	P	
18	VDD	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	C	
19	VPP	FOR TEST	P	
20	VSH1	Positive Source driving voltage	C	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH1	C	
22	VSL	Negative Source driving voltage	C	
23	VGL	Power Supply pin for Negative Gate driving voltage VCOM and VSL	C	
24	VCOM	VCOM driving voltage	C	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output),
P = Power Pin, C =Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU in 4 -wire SPI mode. When the pin is pulled High, the data at SDA will be interpreted as data. When the pin is pulled Low, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI+0.5	V
Logic Output voltage	VOUT	-0.5 to VCI+0.5	V
Operating Temp range	TOPR	0 to +40	°C
Storage Temp range	TSTG	-25 to+70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note: Maximum ratings are those values beyond which damages to the device may occur.
Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	VSS	-		-	0	-	V
Logic supply voltage	VCI	-	VCI	2.2	3.0	3.7	V
Core logic voltage	VDD		VDD	1.7	1.8	1.9	V
High level input voltage	VIH	-	-	0.8 VCI	-	-	V
Low level input voltage	VIL	-	-	-	-	0.2VCI	V
High level output voltage	VOH	IOH = -100uA	-	0.9 VCI	-	-	V
Low level output voltage	VOL	IOL = 100uA	-	-	-	0.1VCI	V
Typical power	PTYP	VCI =3.0V	-	-	TBD	-	mW
Deep sleep mode	PSTPY	VCI =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	VCI =3.0V	-	-	TBD	-	mA
Image update time	-	25 ºC	-	-	12		sec
Sleep mode current	Islp_VCI	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_VCI	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes:1.The typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.

2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

6.3 AC Characteristics

6.3.1 MCU Interface selection

The pin assignment at different interface mode is summarized in Table.Different MCU mode can be set by hardware selection on BS1 pins.The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

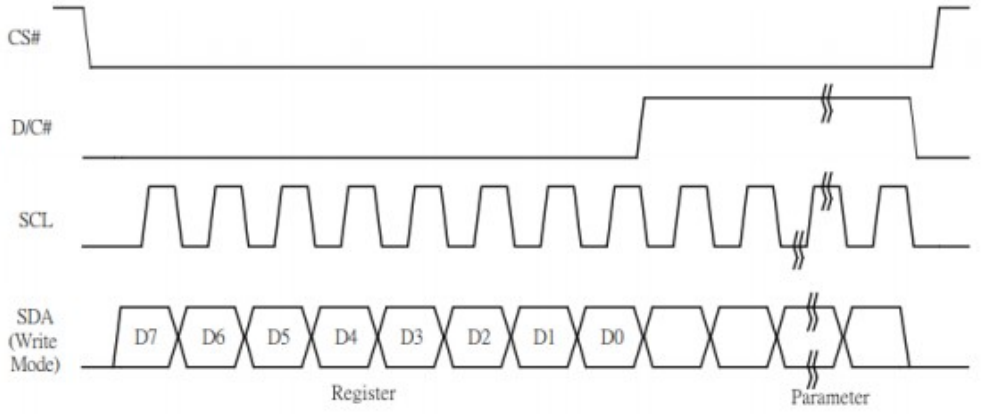
6.3.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#.
This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note:
(1) ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.



Write procedure in 4-wire SPI mode

In the Read mode:

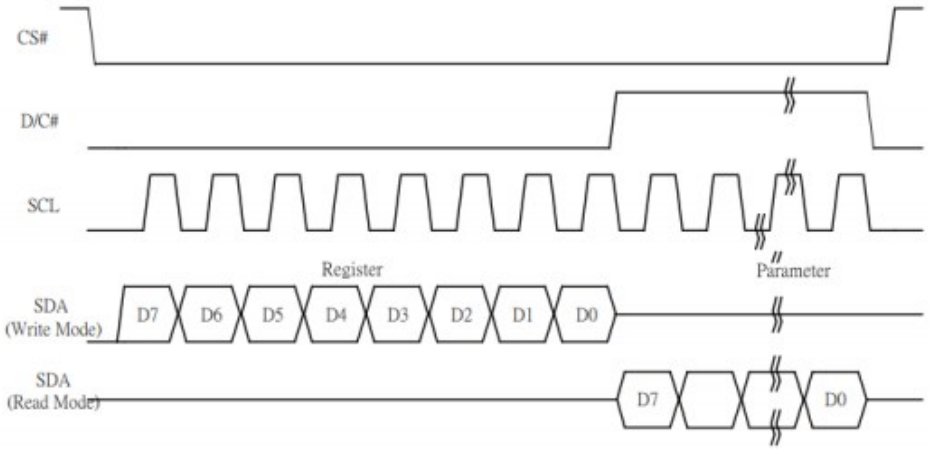
1.After driving CS# to low, MCU need to define the register to be read.

2.SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7,D6,...D0 With D/C# keep low.

3.After SCL change to low for the last bit of register, D/C# need to drive to high.

4.SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7,D6,…D0.

5.Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.



Read procedure in 4-wire SPI mode

6.3.3 MCU Serial Interface (3-wire SPI)

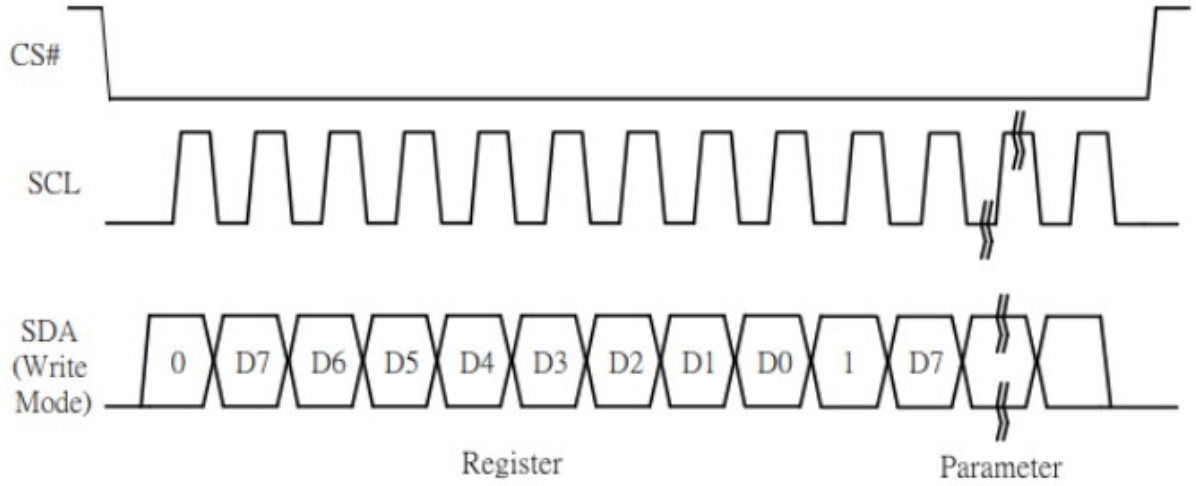
The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#.

This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used.There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence:D/C#bit,D7 to D0 bit.The D/C# bit(first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal



Write procedure in 3-wire SPI mode

In the Read mode:

1.After driving CS# to low, MCU need to define the register to be read.

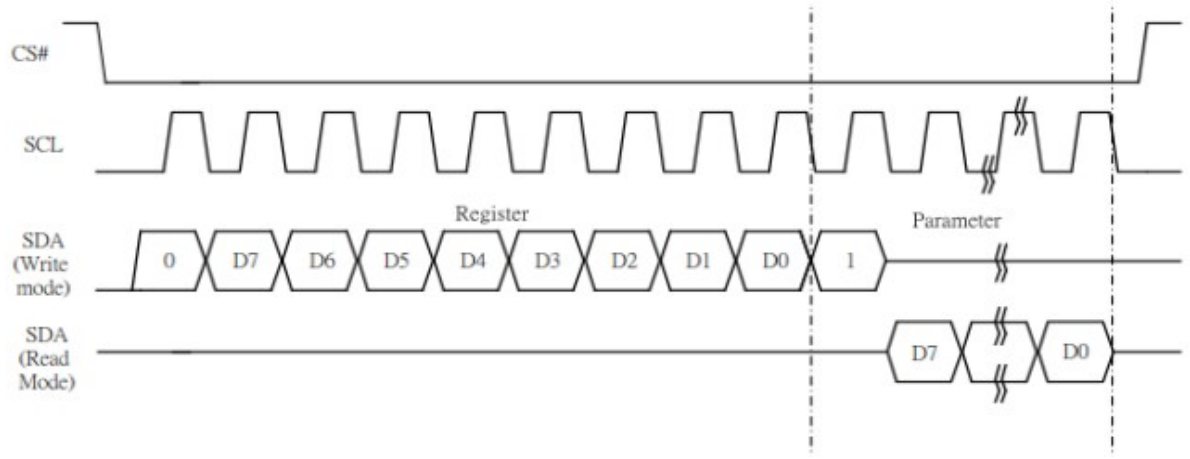
2.D/C=0 is shifted thru SDA with one rising edge of SCL.

3.SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7,D6,...D0.

4.D/C=1 is shifted thru SDA with one rising edge of SCL

5.SDA is shifted out an 8-bit data one very falling edge of SCL in the order of D7,D6,…D0.

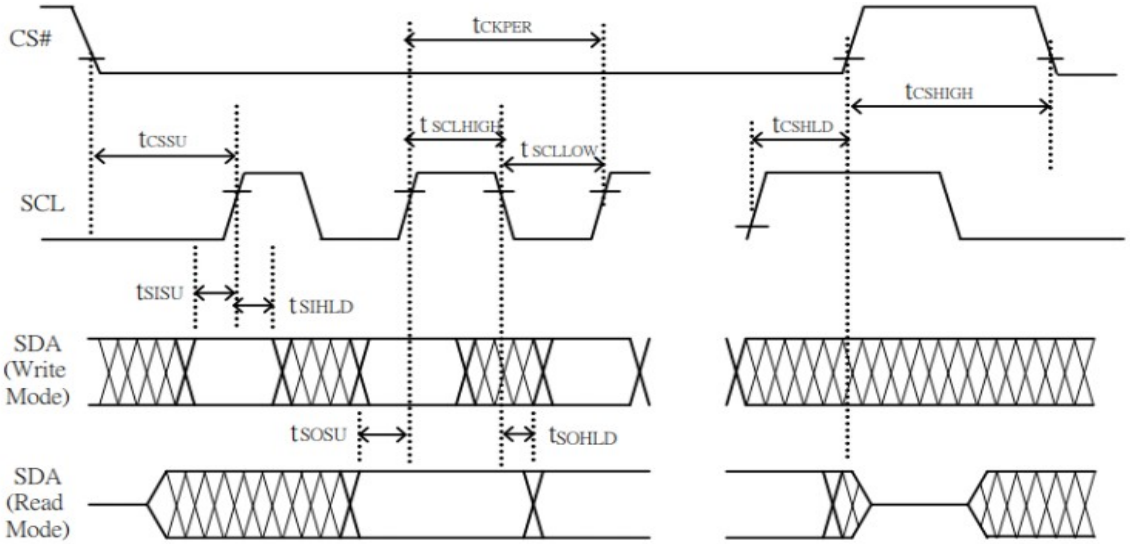
6.Depending on register type, more than 1 byte can be read out. After all byte are read,CS# need to drive to high to stop the read operation.



Read procedure in 3-wire SPI mode

6.3.4 Interface Timing

The following specifications apply for:VSS=0V, VCI=3.0V, TOPR=25ºC



Serial interface Timing Characteristics

(VCI - VSS =2.2V to 3.7V, TOPR = 25℃， CL = 20pF)

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)			20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	60			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	65			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)			2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

7. Optical Characteristics

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	7-1
CR	Contrast Ratio	Indoor	8.1		-		7-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			7-3
T update	Image update time	at 25 °C		12	-	sec	

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

7-3 WS: White state, DS: Dark state

8. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact withelectrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases,which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. Theglass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

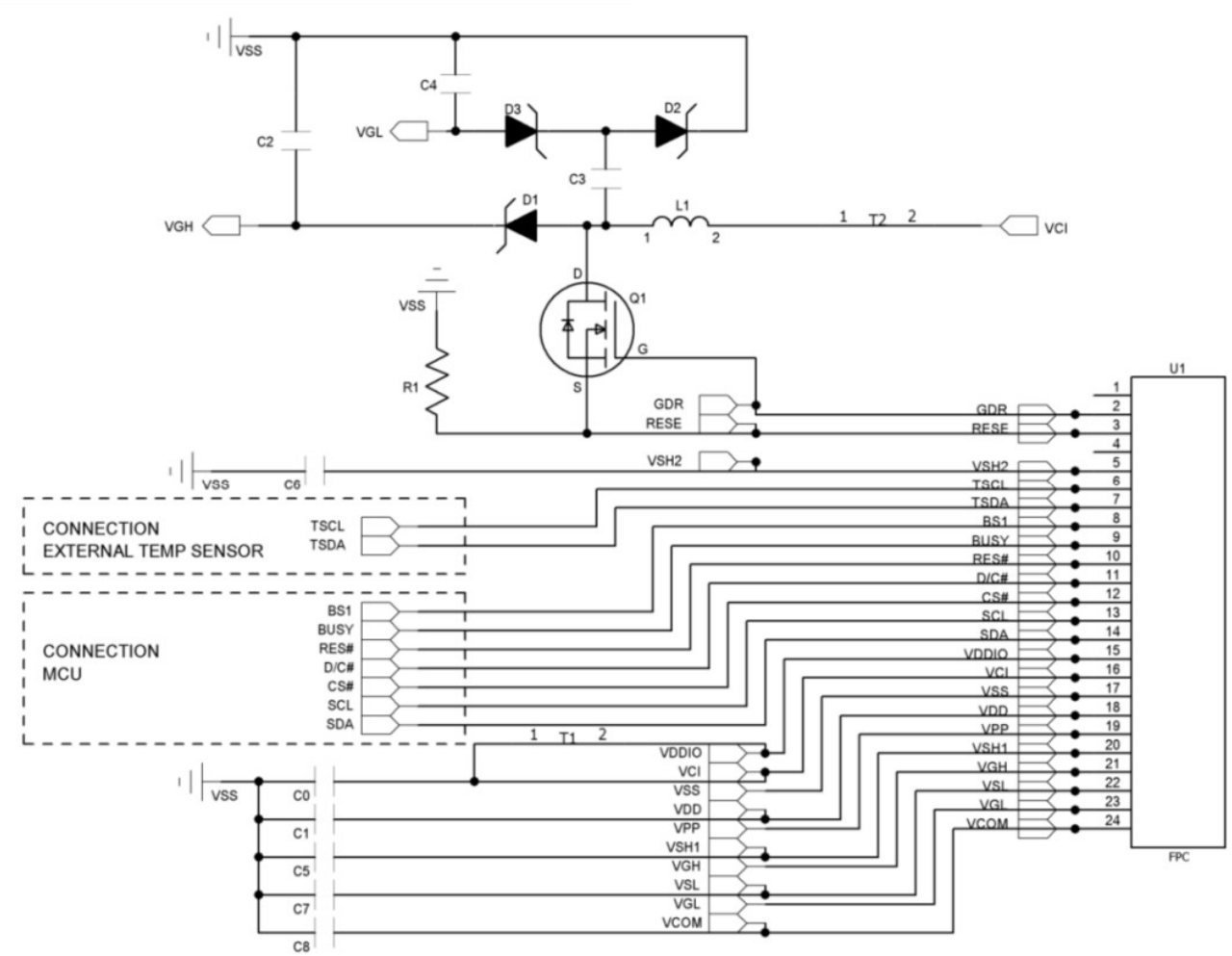
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System(IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device.These are stress ratings only and operation of the device at these or at any other Conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

9. Reliability test

NO.	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70ºC，RH=40%，240 h Test in white pattern
3	High-Temperature Operation	T=40ºC，RH=35%，240 h
4	Low-Temperature Operation	0ºC，240h
5	High-Temperature, High-Humidity Operation	T=40ºC，RH=80%，240 h
6	High Temperature, High Humidity Storage	T=50ºC，RH=80%,240 h Test in white pattern
7	Temperature Cycle	1cycle:[-25°C 30min]→[+70°C 30min]: 50cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs, 40°C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display,no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display,including IC and FPC area)

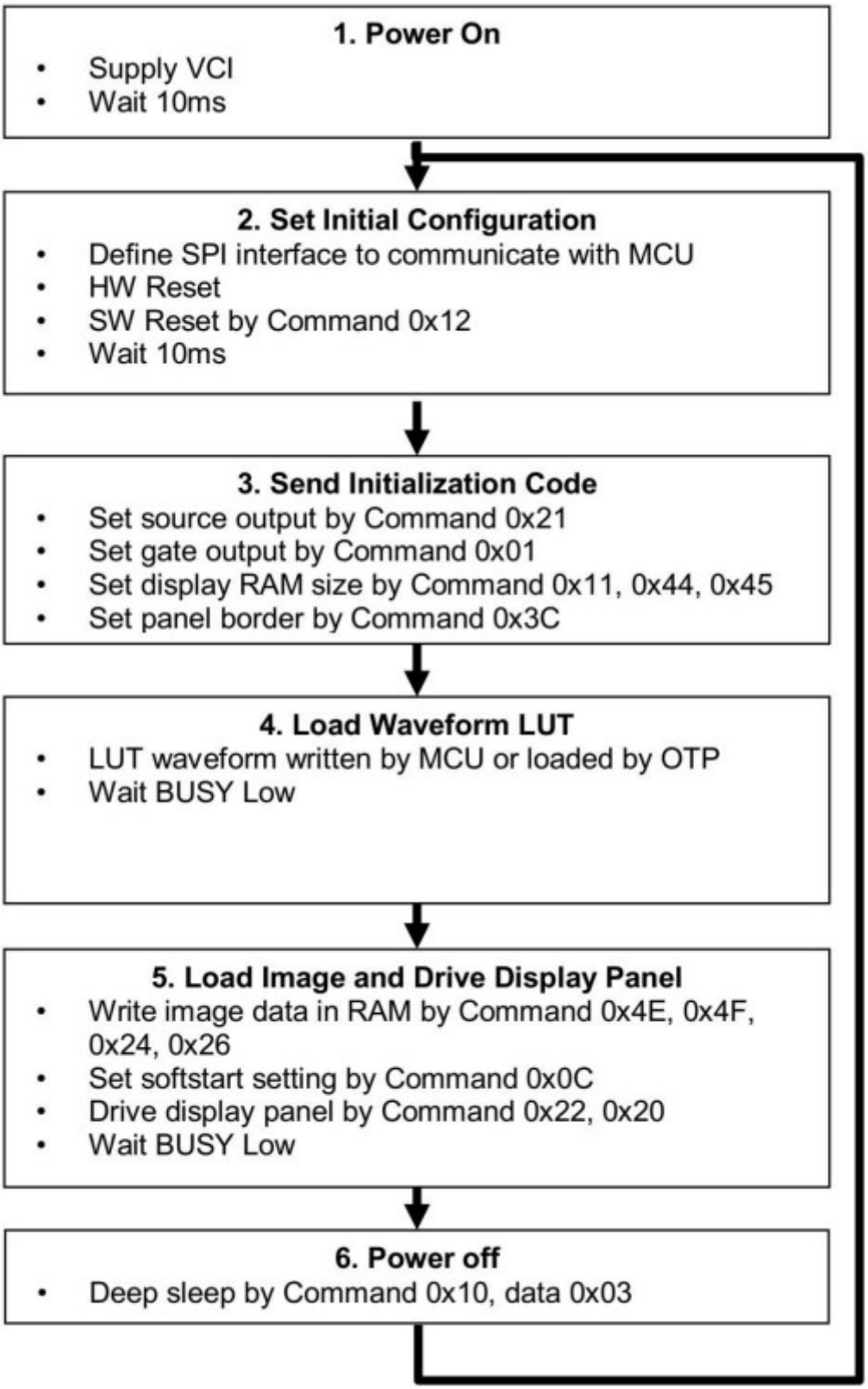
Note:Put in normal temperature for 1 hour after test finished, display performance is ok.

10. Typical Application Circuit with SPI Interface



Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

11. Typical Operating Sequence



12. Inspection condition

12.1 Environment

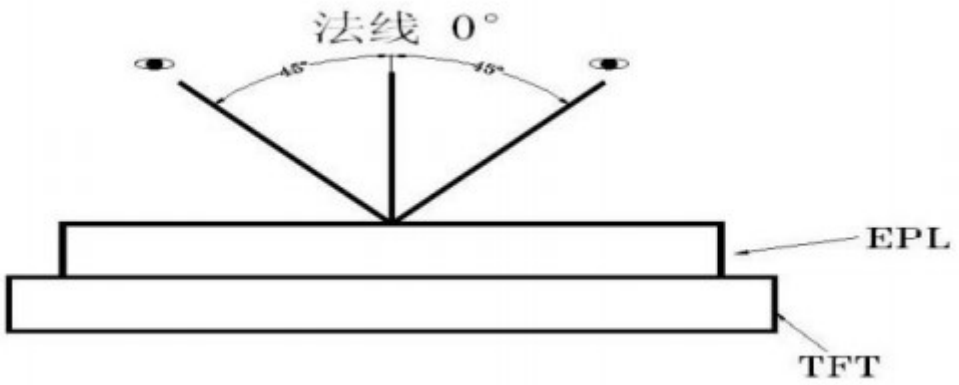
Temperature： 25±3 ℃

Humidity：55±10%RH

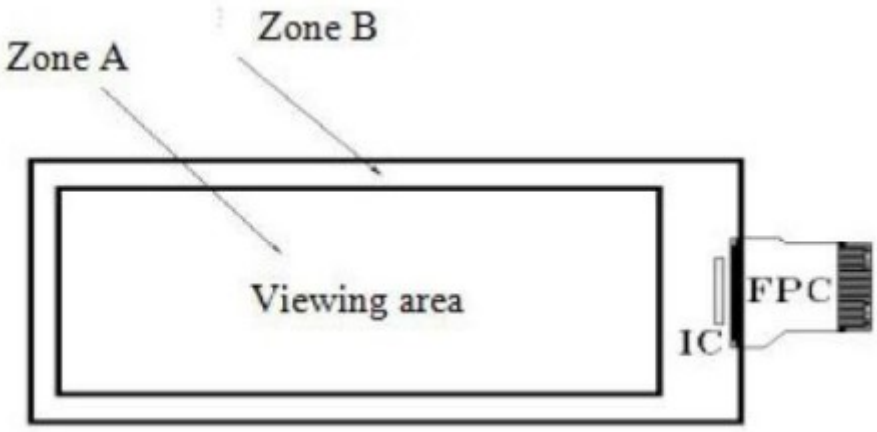
12.2 Illuminance

Brightness:1200～1500LUX; distance: 30CM; Angle: Relate 45°surround.

12.3 Inspect method

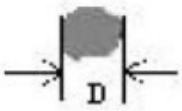
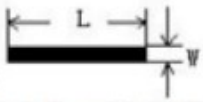


12.4 Display area

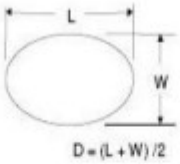
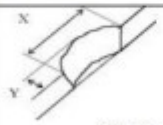
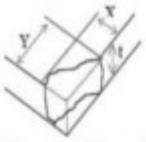
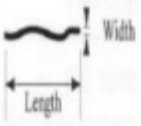


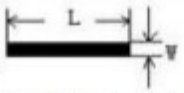
12.5 Inspection standard

12.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm。N≤3， 0.5mm＜D Not Allow	MI		
3	Black/White spots (No switch)	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm，N≤5 D＞0.5mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 L≤1.0mm,W≤0.15mm negligible 1.0mm<L≤4.0mm 0.15mm<W≤0.5mm N≤4 allowable L>4.0mm ,W>0.5mm is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	D≤0.25mm, allow 0.25mm<D≤0.4mm ,n≤4 allow D>0.4mm is not allowed (n≤8 items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤5	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Zone B
14	Silicon glue	Thickness ≤ PS surface(With protect film): Full cover the IC; Shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 t≤1.5mm	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13. Packaging